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Specifications

(54) [Title of the Invention] Semiconductor Single Crystal and Manufacturing Method Thereof

(57) [Summary]
[Object] The objects of the present invention are to provide a silicon single crystal that has excellent oxide layer breakdown voltage (referred to hereinafter as oxide layer breakdown voltage) manufactured by the Czochralski method (referred to hereinafter as the CZ method) and a production method for such single crystal.

[Composition of the Invention] In order to attain the above mentioned goals, manufacture of silicon single crystal by the Czochralski method according to the present invention is carried out such that the crystal is resident within a 1200°C to 850°C temperature region within the furnace for at least 200 minutes. Moreover, the silicon single crystal produced by the present invention has excellent oxide layer breakdown voltage as indicated by an oxide layer breakdown voltage characteristic C mode pass rate per wafer of at least 60%.

[Scope of the Patent Claims}
[Claim 1] A silicon single produced by the Czochralski method such that the crystal is resident within a 1200°C to 850°C temperature region within the crystal grown furnace for at least 200 minutes.

[Claim 2] A method for production of silicon single crystal having excellent oxide layer breakdown characteristics as indicated by an oxide layer breakdown voltage characteristic C mode pass rate per wafer of at least 60% as determined upon a silicon wafer sliced from the single crystal upon which are formed numerous MOS diodes, each as a 5 mm two-layer gate electrode comprising an upper layer of aluminum and a lower layer of doped polysilicon, and pass rate is determined by the count of MOS diodes showing a mean electrical field of at least 8.0 MV/cm across the oxide layer when a current density of 1 microA/cm^2 flows through the oxide layer divided by the total count of MOS diodes.

[Detailed Explanation of the Invention]
[0001]
[Field of Industrial Use]
The present invention relates to a silicon single crystal and production method thereof by the Czochralski method (referred to hereinafter as the CZ method); wherein the silicon single crystal has

excellent breakdown voltage characteristics of the oxide layer (referred to hereinafter as oxide layer breakdown characteristics).

[0002]

[Conventional Technology]

CZ silicon single crystal has conventionally been widely used as material for LSI since such single crystal is characterized as having excellent crystal strength. However, silicon single crystal oxide layer breakdown voltage is known to vary greatly according to fundamental differences in the production method. Oxide layer breakdown voltage of the single crystal wafer produced by the CZ method is markedly low in comparison to single crystal produced by the float zone method and single crystal produced by growth of an epitaxial growth upon CZ single crystal. However, in recent years in accompaniment with the increased degree of integration of MOS devices, there has been strong demand for improved reliability of the gate oxide layer, and development of a production method for CZ silicon single crystal that has an excellent oxide layer breakdown voltage characteristic, as one important characteristic indicating reliability of the oxide layer, is seen as quite important.

[0003] Publication of Unexamined Patent Application No. Hei 2-2671695 discloses a method for production of silicon single crystal of at least 100 mm diameter by the CZ method to produce CZ single crystal that has excellent oxide layer breakdown voltage. This method is characterized by a crystal growth rate of 0.8 mm/minute or less. However, this method is unrealistic due to low productivity. Therefore, although a method has become necessary for production of CZ silicon crystal with excellent oxide layer breakdown voltage at the conventional crystal production rate of 1.2 mm/minute, no such method has existed. [*TRANSLATOR'S NOTE: The patent number in the source text is clearly in error. This should have been 2-267195.*]

[0004]

[Problems to be Solved by the Invention] The objects of the present invention are to provide silicon single crystal by the CZ method that has good oxide layer breakdown voltage and to provide a method for production of such crystal.

[0005]

[Means to Solve the Problems] The present invention, in order to attain the above mentioned objects, is a silicon single produced by the Czochralski method such that the crystal is resident within a 1200°C to 850°C temperature region within the crystal grown furnace for at least 200 minutes.

[0006] Moreover, the present invention is a method for production of silicon single crystal having excellent oxide layer breakdown characteristics as indicated by an oxide layer breakdown voltage characteristic C mode pass rate per wafer of at least 60% as determined upon a silicon wafer sliced from the single crystal upon which are formed numerous MOS diodes, each as a 5 mm two-layer gate electrode comprising an upper layer of aluminum and a lower layer of doped polysilicon, and pass rate is determined by the count of MOS diodes showing a mean electrical field of at least 8.0 MV/cm across

the oxide layer when a current density of 1 microA/cm^2 flows through the oxide layer divided by the total count of MOS diodes.

[0007]

[Operation of the Invention] The present invention will be explained using figures. Figure 1 shows a cross section of a MOS diode upon a silicon wafer obtained by the production method of the present invention for evaluation of oxide layer breakdown voltage. A silicon oxide layer 2 is formed upon a silicon wafer 1. Upon this silicon wafer 1 is formed a two-layer gate electrode 5 of 5 mm diameter comprising an aluminum 1 upper layer and a lower layer formed from doped polysilicon 4.

[0008] Means for evaluation of oxide layer breakdown voltage of the silicon single crystal obtained by the production method of the present invention will next be explained using Table 1.

[0009]
Table 1

No.	Step	Conditions
1	wafer wash	60 seconds immersion in 1.5 wt% HF, followed by ultrapure water rinse
2	gate oxidation	high temperature oxidation at 1000°C in dry oxygen to form about 250 Å thick oxide layer
3	polysilicon layer deposition	640°C deposition temperature, non-doped polysilicon layer, 5000 Å thick
4	pre-oxidation wash	5 minutes immersion at 100°C in 97% H_2SO_4 and H_2O_2 (3:1 volume ratio), followed by rinse in ultrapure water, followed by immersion for 60 seconds in 1.5 wt% HF, followed by rinse in ultrapure water
5	polysilicon oxidation	high temperature oxidation at 900°C in dry oxygen to form about 300 Å thick oxide layer
6	ion implantation	n-type : P doped at 5×10^{15} cm^{-2}, acceleration voltage of 30 keV; p-type : B doped at 10^{16} cm^{-2}, acceleration voltage of 80 keV
7	pre-anneal wash	5 minutes immersion at 100°C in 97% H_2SO_4 and H_2O_2 (3:1 volume ratio), followed by rinse in ultrapure water, followed by immersion for 60 seconds in 1.5 wt% HF, followed by rinse in ultrapure water
8	drive-in anneal	30 minutes in nitrogen at 900°C
9	polysilicon layer etching	in mixture of 40% NH_4F : 50% HF at 10 : 1 volume ratio
10	Al evaporation-attachment	resistance heating evaporation-attachment, 2000 - 5000 Å
11	lithography	positive resist, 1 μm thick
12	Al etching	in mixture of 85% H_3PO_4 : 70% HNO_3 at 19 : 1 volume ratio
13	polysilicon etching	reactive plasma etching, CF_4
14	resist removal	C washing (J100 at 100°C for 10 minutes × 2, in trichloroethylene at 86°C for 5 minutes × 2, in trichloroethylene at 86°C for 10 minutes × 1, followed by infrared drying)
15	hydrogen anneal	in H_2 (2×10^3 cc/minute) + N_2 (10×10^3 cc/minute) at 400°C for 30 minutes
16	resist application	2 μm resist thickness
17	backside polysilicon etching	reactive plasma etching, CF_4
18	resist application	2 μm resist thickness
19	backside polysilicon oxide layer etching	in mixture of 40% NH_4F : 50% HF at 10 : 1 volume ratio
20	backside electrode evaporation-attachment	electron bombardment heating, about 2000 Å thickness, p-type = Au, n-type = AuSb
21	resist removal	C washing (J100 at 100°C for 10 minutes × 2, in trichloroethylene at 86°C for 5 minutes × 2, in trichloroethylene at 86°C for 10 minutes × 1, followed by infrared drying)
22	evaluation of oxide layer breakdown voltage characteristics	voltage ramping method

[0010] The CZ silicon ingot first undergoes typical silicon wafer processing comprising slicing, lapping, polishing, etc. to obtain a wafer. The obtained wafer is washed (1), and gate oxidation is carried out to form a SiO_2 layer (2). A polysilicon layer is deposited (3). Then this polysilicon is doped by ion implantation (6). Oxidation pre-washing (4) and polysilicon oxidation (5) are pre-treatments prior to ion implantation (6). Then pre-anneal washing is performed (7). Drive-in annealing is used to fix dopant

within the polysilicon (8). The polysilicon oxide layer is removed by etching (9). An aluminum layer is formed by vaporization-attachment of aluminum (10). Thereafter a positive resist film is applied and patterned during lithography (11) in order to form two-layer gate electrodes of 5 mm diameter. Thereafter the aluminum layer is etched (12), the polysilicon layer is etched (13), and then the resist layer is removed (14). Finally after hydrogen annealing to stabilize the Si-silicon oxide interface (15), a resist layer is applied to the surface to protect the MOS diodes (16), and plasma etching is used to remove the backside polysilicon layer (17). A protective resist layer is again applied to the surface (18), and the backside oxide layer is removed by etching (19). A backside electrode is formed by evaporation-attachment of gold (in the case of p-type) or gold-antimony alloy (in the case of n-type) (20). Finally, after removal of the protective resist layer (21), the voltage ramping method is used to evaluate oxide layer breakdown voltage characteristics (22). The voltage ramping method is taken to mean a method for the step-wise application of DC voltage over time as an applied current flows between aluminum layer 3 and the backside electrode to inject numerous carriers from the substrate. For the present invention, the per-step voltage increase of this voltage ramping method is 0.25 MV/cm, and the holding time period is 200 ms/step. The proportion (referred to as the C mode pass rate) of individual MOS diodes showing a mean electrical field of at least 8.0 MV/cm in silicon oxide layer 2 when current density through silicon oxide layer 2 of Figure 1 reaches 1.0 $\mu A/cm^2$ is used to evaluate oxide layer breakdown voltage characteristics of the silicon single crystal. The C mode pass rate of silicon single crystal of the present invention is good at a value of at least 60%.

[0011] Fine oxygen precipitates are formed during production within silicon single crystal produced by the CZ method. These fine precipitates exist at the crystal surface and are taken up within the oxide layer during gate oxide layer formation, thereby causing breakdown of insulation to a value of 8 MV/cm or below and reducing C mode pass rate.

[0012] The inventors of the present invention, as a result of detailed investigation into cooling conditions during growth of crystals having various types of oxide layer breakdown voltage characteristics, discovered the following relationship between the formation of fine oxygen precipitates (origin of insulation breakdown) and cooling conditions. That is to say, during the silicon single crystal growth process by the CZ method, fine oxygen precipitate growth nuclei are introduced at the high temperature region between the melting point and 1300°C. Within the 1300°C to 1200°C temperature region, these fine oxygen precipitate growth nuclei are formed. On the other hand, within the 1200°C to 850°C temperature region, these fine oxygen precipitate growth nuclei decompose so that density decreases. In the temperature region of 850°C and below, oxygen precipitation proceeds centered upon the growth nuclei such that fine oxygen precipitates grow.

[0013] When the density of these fine oxygen precipitates is less than or equal to 1×10^5 cm^{-3}, even though such fine oxide precipitates exist in the gate oxide layer formation region of the wafer outer surface, the oxide layer breakdown voltage isn't adversely affected. Therefore although fine oxygen

precipitates adversely affect breakdown voltage, a density of 1×10^5 cm^{-3} or less indicates a silicon single crystal that has good oxide layer breakdown voltage.

[0014] Since CZ silicon single crystal produced by the conventional method resides for only a short time period in the temperature region of 1200°C to 850°C, fine oxygen precipitate generation nuclei formed in the 1300°C to 1200°C temperature region can't decompose sufficiently, thereby causing fine oxygen precipitates to exist at a concentration of at least 1×10^5 cm^{-3} and causing a decrease in the oxidation layer breakdown voltage C mode pass rate.

[0015] However, during silicon single crystal production by the CZ method, by maintenance for at least 200 minutes in the crystal growth furnace in the temperature range of 1200°C to 850°C, a silicon single crystal can be produced that has a good oxidation layer breakdown voltage. The CZ silicon single crystal produced by this method has an oxide layer breakdown voltage C mode rate of at least 60% independent of crystal position, thereby indicating a good oxide layer breakdown voltage.

[0016]
[Working Examples]

Although the working examples of the present invention are explained below, the present invention is not limited by these working examples. Also oxide layer breakdown voltage was evaluated by determination of C mode pass rate by the steps of Table 1 as explained earlier.

[0017] Working Example 1

No particular limitation is placed upon the single crystal production apparatus used for the present invention as long as this is used for silicon single crystal production by the conventional CZ method. A production apparatus such as that shown in Figure 2 was used for the present working example. This CZ method type silicon single crystal production apparatus 11 has a chamber comprising a heat chamber 12a containing a structure for melting silicon and a contiguous pull chamber 12b for containing the grown silicon single crystal ingot S. Heat chamber 12a is divided from pull chamber 12a by an separation mechanism 30. Within heat chamber 12a are provided a crucible 15 comprising a quartz crucible 15b held by a graphite crucible 15a, a heater 16 placed surrounding the perimeter surface of crucible 15, and an insulator 21 for prevention of loss of heat from heater 16 to the heat chamber 12a exterior. This crucible 15 is connected to a non-illustrated drive and a rotation shaft 14. This crucible 15 is rotated at a certain rate by this drive while crucible 15 is raised and lowered in order to prevent lowering of the silicon melt surface in accompaniment with decrease of the silicon melt within crucible 15. A pull cable 17 is provided hanging vertically down within pull chamber 12b. A chuck 19 for holding a seed crystal 18 is provided at the bottom tip of this cable. This pull cable 17 is wound up by a cable winding mechanism 20 so that the silicon single crystal ingot is pulled up. Ar gas is fed from gas feed port 22 formed within this pull chamber 12b. This gas flows throughout the interior of heat chamber 12a and discharges through gas flow port 23. This type of discharge of Ar gas prevents mixing into the silicon melt of SiO generated within the chamber by melting of silicon.

[0018] Silicon single crystal was grown using this apparatus under the conditions listed below.

Precursor material melt weight: 45 kg
Single crystal growth rate: 1.2 mm/minute
Time period in 1200°C - 850°C temperature range: 210 minutes

The following silicon single crystal ingot was grown under these conditions.

Conductivity type: p-type (boron doped)
Crystal diameter: 6 inch type (160 mm)
Resistivity: 10 Ω·cm
Oxygen concentration: $7.5 - 8 \times 10^{17}$ atoms/cc
(calculated using oxygen concentration conversion coefficient according to the Japan Electronics Industry Development Association)
Carbon concentration: $< 1.0 \times 10^{17}$ atoms/cc
(calculated using carbon concentration conversion coefficient according to the Japan Electronics Industry Development Association)

Oxide layer breakdown voltage of wafers sliced from this ingot was measured as shown in Table 2. As shown by Table 2, oxide layer breakdown voltage C mode pass rates for these silicon wafers were all at least 60%, indicating that wafers sliced from silicon ingot produced by the method of the present invention had good oxide layer breakdown voltage.

[0019] Working Example 2

Silicon single crystal was grown under the conditions listed below using the apparatus of working example 1.

Precursor material melt weight: 45 kg
Single crystal growth rate: 1.5 mm/minute
Time period in 1200°C - 850°C temperature range: 400 minutes

The following silicon single crystal ingot was grown under these conditions.

Conductivity type: n-type (phosphorous doped)
Crystal diameter: 6 inch type (160 mm)
Resistivity: 2 Ω·cm
Oxygen concentration: $9.8 - 10.0 \times 10^{17}$ atoms/cc
(calculated using oxygen concentration conversion coefficient according to the Japan Electronics Industry Development Association)
Carbon concentration: $< 1.0 \times 10^{17}$ atoms/cc
(calculated using carbon concentration conversion coefficient according to the Japan Electronics Industry Development Association)

Oxide layer breakdown voltage of wafers sliced from this ingot was measured as shown in Table 2. As shown by Table 2, oxide layer breakdown voltage C mode pass rates for these silicon wafers were all at least 60%, indicating that wafers sliced from silicon ingot produced by the method of the present invention had good oxide layer breakdown voltage.

[0020] Comparative Example 1

Silicon single crystal was grown under the conditions listed below using the apparatus of working example 1.

Precursor material melt weight: 45 kg
Single crystal growth rate: 1.2 mm/minute
Time period in 1200°C - 850°C temperature range: 190 minutes

The following silicon single crystal ingot was grown under these conditions.

Conductivity type: p-type (boron doped)
Crystal diameter: 6 inch type (160 mm)
Resistivity: 10 Ω·cm
Oxygen concentration: $7.5 - 7.8 \times 10^{17}$ atoms/cc
(calculated using oxygen concentration conversion coefficient according to the Japan Electronics Industry Development Association)
Carbon concentration: $< 1.0 \times 10^{17}$ atoms/cc
(calculated using carbon concentration conversion coefficient according to the Japan Electronics Industry Development Association)

Oxide layer breakdown voltage of wafers sliced from this ingot was measured as shown in Table 2 together with working example 1 and working example 2. As shown by Table 2, oxide layer breakdown voltage C mode pass rates for these silicon wafers were all less than 60%, indicating that oxide layer breakdown voltage wasn't superior.

[0021] Comparative Example 2

Silicon single crystal was grown under the conditions listed below using the apparatus of working example 1.

Precursor material melt weight: 45 kg
Single crystal growth rate: 1.5 mm/minute
Time period in 1200°C - 850°C temperature range: 100 minutes

The following silicon single crystal ingot was grown under these conditions.

Conductivity type: n-type (phosphorous doped)
Crystal diameter: 6 inch type (160 mm)
Resistivity: 2 Ω·cm
Oxygen concentration: $9.8 - 10.0 \times 10^{17}$ atoms/cc
(calculated using oxygen concentration conversion coefficient according to the Japan Electronics Industry Development Association)
Carbon concentration: $< 1.0 \times 10^{17}$ atoms/cc
(calculated using carbon concentration conversion coefficient according to the Japan Electronics Industry Development Association)

Oxide layer breakdown voltage of wafers sliced from this ingot was measured as shown in Table 2 together with working example 1, working example 2, and comparative example 1. As shown by

Table 2, oxide layer breakdown voltage C mode pass rates for these silicon wafers were all less than 60%, indicating that oxide layer breakdown voltage wasn't superior.

[0022]
[Table 2]

	C mode pass rate
Working example 1	88%
Working example 1	82%
Working example 1	85%
Working example 2	90%
Working example 2	92%
Working example 2	91%
Comparative example 1	28%
Comparative example 1	32%
Comparative example 1	26%
Comparative example 2	11%
Comparative example 2	5%
Comparative example 2	8%

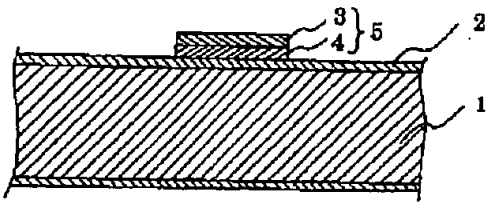
[0023]
[Results of the Invention] The silicon single crystal of the present invention and the silicon single crystal obtained by the production method of the present invention are appropriate for a wafer used for MOS devices that has high gate oxide layer reliability due to a good oxide layer breakdown voltage.

[0024]
[Simple Explanation of the Figures]
[Figure 1] This is a partial cross-sectional drawing of a MOS diode formed upon a silicon wafer for evaluation of oxide layer breakdown voltage characteristics of silicon single crystal of the present invention.
[Figure 2] This is a schematic drawing showing the CZ method type silicon single crystal production apparatus used in the working examples of the present invention.

[Explanation of Items]
1 .... silicon single crystal
2 .... insulation oxide layer
3 .... aluminum layer
4 .... polysilicon layer
5 .... two-layer gate electrode
11 .... CZ method silicon single crystal production apparatus
12 .... chamber

12a	....	heat chamber
12b	....	pull chamber
14	....	rotation shaft
15	....	crucible
15a	....	graphite crucible
15b	....	quartz crucible
16	....	heater
17	....	cable
19	....	chuck
20	....	cable winding mechanism
21	....	insulation
22	....	gas feed port
23	....	gas discharge port
30	....	separation mechanism

[Figure 1]



[Figure 2]